IN THE SPECIFICATION:

Please amend paragraph [0010] as follows:

FIG. 8 is a plan view of a conventional reticle 81 on which patterns of a product chip are arranged. As shown in FIG. 8, the reticle 81 has a plurality of device patterns 83-1 to 83-4 formed in an exposure area (wafer transfer area) exposed by an exposure apparatus. The device patterns 83-1 to 83-4 are respectively those related to the product chip, [[and]] all of which are identical. Outside an exposure area 82 on the reticle 81, alignment patterns 84 used for positional adjustment of the reticle during the light exposure are arranged. Label areas 85 are those for placing the identification numbers or the like of the reticle.

Please amend paragraph [0013] as follows:

Whether any defect in the pattern was detected or not by the defect inspection is then judged (step S84). If any defect was detected, the defect is then judged whether it is a substantial defect located on the pattern or not, that is, whether the detected defect should necessarily be corrected or not (step S85). On the other hand, if it was judged in step S84 that no defect was detected, the process comes to [[the]] an end.

Please amend paragraph [0015] as follows:

If the defect confirmation on the reticle comes to [[the]] an end, or if there is no need of additional defect confirmation, the process will be terminated, but if not, the process will be

returned to step S84 (step S87).

Please amend paragraph [0018] as follows:

In some conventional product reticles, a pattern identical to the device pattern of the product chip formed in the exposure area, or a part of the device pattern is formed on the reticle as a collation pattern used for comparison with the device pattern, separately from such device pattern (see Japanese Patent Application Laid-Open No. Sho 63-163464 and Japanese Patent Application Laid-Open No. Hei 1-244304, for example), for use in the above-described comparative inspection (step S83 in FIG. 7B) for detecting any defect. In the defect inspection of the reticle, the presence or absence of the defect is inspected by comparing the device pattern of the product chip, and by confirming the identity therebetween.

Please amend paragraph [0032] as follows:

The conventional reticle inspection, however, is disadvantageous in that the inspection cannot be made under the same ~~condition~~ conditions because of ~~difference~~ differences in the inspection wavelength and exposure wavelength; that the pattern formed on the reticle and the pattern transferred onto the semiconductor wafer are different in size; and that the operator has to comparatively observe the images; all of these make it rather difficult to judge whether or not the defects are in need of correction ~~or not~~, and in some cases, even result in discovery of non-conformities only after the defect inspection.

Please amend paragraph [0033] as follows:

Another problem in some conventional reticle ~~inspection~~ inspections resides in that all detected defects having a size larger than a predetermined size are corrected irrespective of their types. This undesirably results in an increase in the number of process steps, because even the defects not affective to the pattern transfer are corrected in the correction process.

Please amend paragraph [0034] as follows:

Although some recent approaches have been made on judgment of whether or not the correction is necessary ~~or not~~ based on simulation, the technique therefor is still on the way to be established.

Please amend paragraph [0042] as follows:

The evaluation reticle has a plurality of representative programmed defects preliminarily arranged thereon in the exposure area (wafer transfer area) 21, for the purpose of confirming transferability of any defect of the reticle onto a semiconductor wafer (transfer target). The programmed defects are patterns formed as preliminarily assumed defects on defect-free patterns (see patterns A0, B0, C0, D0 and F0 shown in FIG. 2B), and are arranged in a plural number by types of the defects (defect types) while ~~being varied~~ varying in size of the defects (defect sizes) on the evaluation reticle. It is to be noted that, in FIG. 2, the pattern portions are indicated by black filling, and on the reticle where glass is used for the substrate, the pattern portions are

composed of chromium which can serve as a light interception film.

Please amend paragraph [0056] as follows:

It is to be understood that FIG. 4A shows only an exemplary case where the evaluation pattern area 44 is disposed on the upper side of the exposure area 42 as viewed in this drawing, and any other area different from the exposure area 42 and at an arbitrary position outside the exposure area 42 on the product reticle 41 [[are] is allowable. The number [[of]] or disposition of the evaluation pattern area 44 is not limited to one but may be two or more, where the evaluation patterns may be disposed on the upper and lower sides of the exposure area 42, or may be on the upper and left sides, for example.

Please amend paragraph [0061] as follows:

The programmed defects arranged herein in the evaluation pattern area 44 are such as those for evaluating the transferability of the defects in the exposure area 42 on the product reticle 41 as described in the above, that is, for evaluating whether the defects can be transferred onto the semiconductor wafer or not when the reticle is exposed by light. It is therefore sufficient for the evaluation pattern area 44 to have, arranged therein as the evaluation pattern, at least the programmed defects A2, B3, C4, D2, E5 and F1 having the largest defect sizes in the individual defect types, out of the programmed defects judged as being untransferable in the above-described preliminary evaluation process, and whether or not other programmed defects are

additionally arranged ~~or not~~ is a matter of arbitrary choice.

Please amend paragraph [0065] as follows:

The defect inspection is carried out based on the defect inspection sensitivity set by step S12. This allows any portion of ~~difference~~ differences in the device patterns 43-1 to 43-4 exceeding the defect inspection sensitivity [[can]] to be detected as ~~defect~~ defects, whereas any portion of ~~difference~~ differences smaller than the defect inspection sensitivity is not judged as defect.